Modeling and Simulation of a Neural Network in Single-Electron Tunneling Technology

C. Gerousis\textsuperscript{1}, J. Martin \textsuperscript{2}

\textsuperscript{1}Department of Physics, Computer Science and Engineering, Christopher Newport University.
\textsuperscript{2}Department of Mathematics, Christopher Newport University, Newport News, VA, USA

Abstract - As the silicon industry transitions into sub-20 nanometer dimensions, major technology challenges in device performance imposed by fundamental physics laws due to scaling become inevitable. Single-Electron Tunneling (SET) transistor is one of several nanoscale devices proposed to overcome the problems that accompany the scaling of the conventional MOS transistor. SET devices offer remarkable features such as small size and potential to operate with very low power supply, which suggests that they could be used in low-power arrays of locally-connected networks ideal for signal and image processing applications. Herein, we first present a SET artificial neural network (ANN) based on threshold logic gate (TLG) paradigm. We then use a Monte Carlo-based simulator to verify the network’s operation in an attempt to realize a number recognition application. We also explore one future direction of SET technology and present a simulation of a hybrid SET-MOS structure. Finally, we end with conclusions and future prospects.

Keywords: Circuit Simulation, Threshold Logic, Nano-Electronics.

1 Introduction

It is generally known that scaling of the current silicon transistor will ultimately reach a limit imposed by the laws of physics [1]. Meeting the challenge of extending scaling beyond roadmap projections may require finding an alternate to the conventional transistor. Among the candidates that can potentially replace the silicon transistor is the SET device [2], which offers striking features such as reduced dimensions, low power consumption, and novel applications. This paper investigates through a circuit simulation study the feasibility of using the SET transistor as a neural network building block. We first present an ANN based on single-electron threshold logic. We then use a Monte Carlo-based simulator to verify the network’s operation in an attempt to realize a number recognition application. We also explore one future direction of SET technology and present a simulation of a hybrid SET-MOS structure. Finally, we end with conclusions and future prospects.

2 SETs in Threshold Logic Gate

In order to efficiently design SET circuits that operate more closely to their natural state at the junction level, we examine one model based on the threshold logic [4]. The SET TLG cell in Fig. 1 consists of multiple capacitive inputs and a single-tunnel junction of 0.1 aF capacitance coupled to the inverter block that acts as the activation function for the ANN. The TLG cell compares the weighted sum of the inputs at ‘+’ node and the threshold value \( \psi \); if the sum is greater or equal to the threshold, the output is logic 1, otherwise the output is logic 0. In the same figure, the capacitively weighted inputs \( V_1-V_2 \) are added to \( V_j \) (the voltage across the tunnel junction) while the weighted inputs of \( V_3-V_4 \) is subtracted from \( V_j \). The threshold can be adjusted by changing the bias voltage \( V_b \), which makes the SET circuit reconfigurable [5].

We use several TLG circuits to construct an ANN network for a number recognition application. The ANN architecture of Fig. 2 contains several layers of hidden operations between input and output. Our TLG ANN architecture, as can be seen in Fig. 3a, includes row detection, number recognition, and number encoding. This paper investigates through a circuit simulation study the feasibility of using the SET transistor as a neural network building block. We first present an ANN based on single-electron threshold logic. We then use a Monte Carlo (MC) simulator to verify the correctness of the network that can be used in an image processing application.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{schematics.png}
\caption{Schematics of a SET threshold-gate-inverter cell.}
\end{figure}
node. As for the 1000 bit pattern TLG, the cell has inputs $V_1$-$V_3$ connected to ‘+’ and $V_4$ attached to node ‘−’ node. For detection of bit pattern 1111, the TLG cell has $V_1$-$V_4$ connected to the ‘−’ nodes. As for the 1000 bit pattern TLG, the cell has inputs $V_1$-$V_3$ connected to ‘+’ and $V_4$ attached to node ‘−’ node. For detection of bit pattern 1111, the TLG cell has $V_1$-$V_4$ connected to the ‘−’ nodes. The simulation results in Fig. 4 show the TLG-inverter output, $V_{out}$ when a bit pattern is detected in an image as 0001, equivalent to pixels □ □ □ □.

The same figure shows $V_{out}$ when a bit pattern is detected as a 1000 image corresponding to pixels □ □ □ □. In our final network, the inputs/output signals are 16 and 0 mV for logic high and low. We note that the input signals $V_1$-$V_4$ are used for the purpose of determining the bit patterns, which specifies the number of capacitance couplings to the ‘+’ and ‘−’ nodes of Fig. 1. After the proper bit pattern is identified by the threshold gate sub-networks, each TLG cell returns a logic high that is sent to the next level, the number recognition.

This stage whose role is to identify the proper combination of bit pattern in a row contains 5-input AND gates for each number represented by the 5x4 matrix. The outputs of the number recognition sub-networks are lastly sent to three SET OR gates that make up the encoder output of the TLG-ANN. We note that all AND and OR SET circuits have similar structure based on the TLG-inverter cell of Fig. 1. The proposed TLG-ANN schematic for number recognition as shown in Fig. 5 can detect pixels of a selected image through the combination of TLG and feedforward connections established by the networks layers. The simulation results confirm that the correct ‘Encoder’ outputs S0, S1 and S2 as encrypted by binary bits 000–111 or numbers 0–7. The ‘Encoder’ output for number ‘5’ is shown in Fig. 6. Our feedforward networks do not require learning as they already operate in a stable state. In addition, the TLG sub-networks have fixed weights established by the capacitor couplings to the SETs, which limits training. In a programmable neural network processor, a training algorithm can be used to adjust the weights in order to perform image processing/recognition. Another limitation to the Monte Carlo simulator used in this study is that it does not allow the user to cut and paste circuit components, nor does it allow the creation of reusable circuit elements. Thus, designing complex circuits can become very time consuming as the designer must lay every component or modify the simulation files at the basic junctions and capacitors level.
2.1 Hybrid SET-MOS

One major downside of SET devices is the low temperature operation so that the thermal fluctuations can be avoided. Since SET devices are winners for their small size, low power dissipation, and new functionality while conventional silicon transistors are the champions for high voltage gain and speed, hybrid SET-MOS architectures may become an attractive option for a future system-on-a-chip. SETs in a hybrid structure with MOS devices can be modeled in Verilog-A, which is "high-level hardware description language (HDL)" of analog systems. One can then combine SmartSpice BSIM device models [6] with Verilog-A modules in the same netlist. We use the SET Verilog-A model [7] to co-simulate the hybrid SET-MOS neuron cell [8] shown in Fig. 7. The current through the SETs is on the order of nanoamperes, which requires MOS bias in subthreshold region. SET device parameters include gate capacitance of 0.04 aF and a tunnel capacitance of 0.02 aF with a tunnel...
resistance of 1MΩ. This simulation approach takes less time in comparison to the Monte Carlo technique. The simulation results of the hybrid neural cell depict the activation function of the neural cell for various offset voltages as shown in Fig. 8. Although the hybrid SET-MOS structures appear to be good candidates for the next electronics generation, it is the difficulty at present time to realize structures with sufficiently small capacitances such that they operate at room temperature. Moreover, device-to-device variations for present structures are quite large which is an issue that has to be overcome by greatly improved process technology or some scheme of self-assembled organization.

![Fig. 7. Hybrid SET-MOS neuron cell.](image)

![Fig. 8. Neural cell activation function. (Reproduced with permission from [7], Copyright IEEE)](image)

### 3 Conclusions

Herein, we discussed the modeling and simulation of a neural network in SET devices based on the threshold logic gate. The TLG-ANN can detect pixels in a selected image and through the combination of TLG and feedforward connections perform the number recognition using the ‘Encoder’ SET block as the output of the network. We also investigated a future direction of SET technology and demonstrated the simulation of a hybrid SET-MOS neural cell, which exhibited the activation function for different offsets. Some of the persisting challenges in realizing SET circuits include the requirement of sophisticated design techniques to overcome the inaccuracies caused by the small size of the nanoscale circuit elements, the low signal levels, and the complexity of connecting the system to the outside world.

### 4 References


